In the Claims

The following listing of the claims replaces all previous listings.

1. (Currently Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells, comprising the operations of:

providing a power supply capacitor cell corresponding to a logic gate cell, a capacitance value of the power supply capacitor cell being determined based on a drive load capacity value of the logic gate cell, and

arranging the power supply capacitor cell in a vicinity of the logic gate cell which is used to determine the capacitance value of the power supply capacitor cell, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell.

2. (Previously Presented) The LSI layout method according to claim 1, wherein the capacitance value of the power supply capacitor cell is determined to be substantially twice as large as the drive load capacity value of the logic gate cell.

3. (Previously Presented) The LSI layout method according to claim 1, wherein the power supply capacitor cell is arranged in the vicinity of the logic gate cell which changes simultaneously with clock synchronization.

4. (Previously Presented) A LSI layout method according to claim 1, further comprising the operations of:

calculating a possible number of the power supply capacitor cells to be arranged based on a width of a dead space of the power supply and a width of the power supply capacitor cells, and

arranging the power supply capacitor cells in spaces of each block where standard cells are not arranged by the automatic arrangement wiring.

5. (Previously Presented) The LSI layout method according to claim 1, wherein the power supply capacitance cell includes:

a p-sub wafer;

a n-well fixed to the ground line on the p-sub wafer, and

a polysilicon gate fixed to the power supply line on the n-well.

6. (Currently Amended) A LSI layout method for a LSI design by automatic arrangement wiring of standard cells, wherein logic gate cells and power supply capacitor cells are provided as the standard cells; comprising the operations of:

providing a power supply capacitor cell corresponding to a logic gate cell, a capacitance value of the power supply capacitor cell being determined based on a drive load capacity value of the logic gate cell, and

arranging the power supply capacitor cell adjacent to the logic gate cell which is used to determine the capacitance value of the power supply capacitor cell, so as to connect a power supply line of the logic gate cell with a ground line of the logic gate cell through the power supply capacitor cell.